FINFET BASED 8T SRAM CELL DESIGN FOR REDUCED READ TIME AND LOW LEAKAGE

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***Abstract*— Scaling down devices has been going on for decades in order to gain greater performance in terms of speed, power consumption, size, and reliability. Data preservation and leakage current reduction are two important concerns in today's memory cells. SRAM (Static Random Access Memory) is a type of memory that is used to store information. SRAM cells in traditional static random access memory (SRAM) suffer from a flaw. Due to their improved performance, power efficiency, and scalability, FinFETs have supplanted planar MOSFETs. Due to physical limitations, process differences, and short-channel effects, even FinFETs are likely to hit their scaling limits. We constructed FinFET-based 8T SRAM cells in this study and compared them to previously reported 6T and 8T SRAM cells. pFin is used in 8T SRAM cells.**

Index Terms ***–8T SRAM,CMOS.***

I. INTRODUCTION

finfets, a type of multigate transistor, have surpassed planar mosfets in terms of performance, short-channel behaviour, and energy efficiency . finfets provide you more control over the channel because they surround it on all sides. this increases the drain-induced barrier-lowering impact, enhances the subthreshold slope, and lowers leakage current. furthermore, finfet by using a weakly doped or undoped channel, you can limit random dopant fluctuations. unfortunately, even with finfets, device scaling is getting increasingly difficult due to lithogra- phy's nearing limits, intolerable short-channel effects, and rising manufacturing costs. other approaches, such as the development of new devices, the use of new integration technologies, the development of new architectures, and the development of novel processing paradigms, are required to aid in the advancement of computing technology.

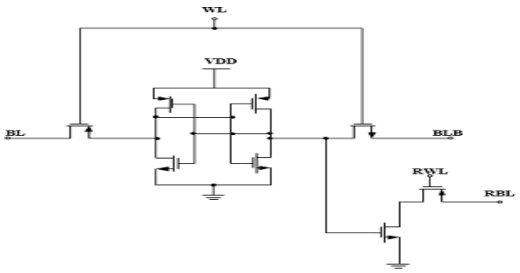
II LITERATURE SURVEY

A comprehensive literature review was conducted, and various technical publications and dissertations were consulted. Some textbooks on VLSI design were also mentioned. The following are a few of the technical articles that were referred to.

1) A Low Level of Leakage Ultra-Low Power Operation with a 9T SRAM Cell In this research, a new 9T cell is presented to achieve read stability while reducing bitline leakage, resulting in lower power consumption than 10T cells. In comparison to a 10T cell employing 32nm CMOS technology, simulation findings reveal that the proposed 9T cell achieves around 18. By considering the three figures of merit of stability, power consumption, and performance, an ideal operating power supply voltage of 0.6V has been identified for the suggested 9T cell. The 9T SRAM cell performs best at this power supply voltage.

2) Design of a Three-Dimensional Monolithic FinFET-Based 8T SRAM Cell with Improved Read Time and Low LeakageThis study introduces two novel 3-D 8T SRAM cells that are implemented in TLM technology and compares them to previous 6T and 8T SRAM cells.To achieve an area-efficient 3-D architecture, the proposed cells use pFinFET access transistors. They have the least leakage current and read time of any cell, as well as great read stability, but poor writeability. To improve writeability, one cell we proposed uses IG FinFETs as pullup transistors with the back gates connected to the supply voltage. This cell reduces the footprint area by 28.1 percent and the leakage current by 31.6 percent, respectively.

Fig 1: 8T CMOS SRAM



III FINFET 8T SRAM

FinFETs have a number of advantages over MOSFETs, including a higher Ion/Ioff ratio. Switching speed is faster, and power consumption is reduced. Furthermore, it has solved the MOSFETs' scalability restrictions. Shorted Gate (SG) mode, Low Power (LP) mode, and Mixed LP-IG mode are the three operating modes of the FinFET. The SG model is similar to a MOSFET, however the LP mode is better suited to low-power applications. In this article, two different types of FinFETs, shorted gate mode and LP-IG mode, are employed to investigate the 8T SRAM. The drive current of the FinFET can be increased by increasing the width of the channel i.e. by increasing the height of the Fin. We can also increase the device drive current by constructing parallel multiple fins connected together as shown in the Figure 2.3. It implies that for a FinFET, the arbitrary channel width is not possible, since it is always a multiple of fin height. So, effective width of the device becomes quantized.

Widthof Channel = 2XFinHeight + FinWidth

N-curve Matric

Drawing butterfly (or VTC) curves of the two back-to-back inverters of the SRAM from a DC simulation to ensure cell stability. However, there are some disadvantages to measuring the SNM using the butterfly

curves (VTC) approach, including the inability to measure the SNM with automatic inline testers and the fact that it takes longer to determine the SNM due to the mathematical calculations or fitting of the squares on each lobe of the VTC curve. Due to systemic mistakes in

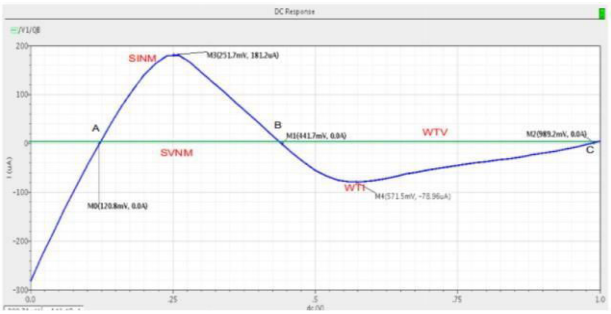


Figure 2:N-Curve

computation, it may not always provide extremely accurate findings. The N-curve metric is used for inline Prior to a change in the cell's content, it is the maximum allowable DC noise voltage at the inverter's input. Thus, the voltage difference between A and B in the simulation figure reflects the maximum allowable DC noise voltage before switching the content of the cell.

$$SVNM = V_B - V_A$$

Write trip voltage

When both bit lines are clamped at Vdd, it is the least voltage drop required to flip the internal node "1" of the SRAM cell. As a result, it can be calculated as the difference between point C and point B. The write ability of an SRAM cell is measured using WTV.

Write trip current

It is measured as a negative peak current between C and B and represents the smallest amount of current required to write the cell. A point A and a point B, or a point B and a point C. WTI is used to characterise the write ability of the SRAM cell, and C stands for loss of SRAM cell stability.

Static noise margin

This is the result of the SVNM and SINM working together. And for improved writing abilities, this value should be high. It is derived from the area below the curve between point A and B.

$$SPNM = \Sigma V \text{ in} * Iin$$

Leakage current

Leakage current is becoming a key source of total power consumption for SRAM cells as CMOS technology continuesto improve. Subthreshold and gate leakage are presently the most common forms of leakage in nanoscaled transistors with low threshold voltages, and this trend continues as technology advances down to 22nm, 16nm, and 10nm nodes. As the channel length is shortened, the MOSFET's threshold voltage decreases. The term "roll-off" refers to the decrease in threshold voltage when the channel length is reduced. As a result, the subthreshold current is bigger. Furthermore, gate leakage caused by variations in oxide thickness, tox, and gate length has a greater impact on NMOS than PMOS.

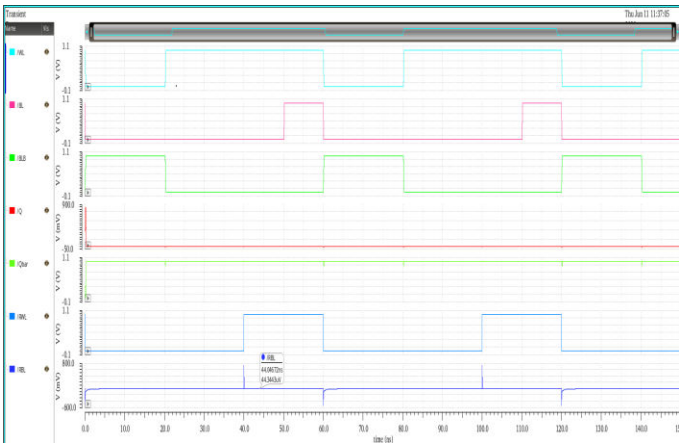
CHALLENGES IN IMPLEMENTATION OF FINFETS

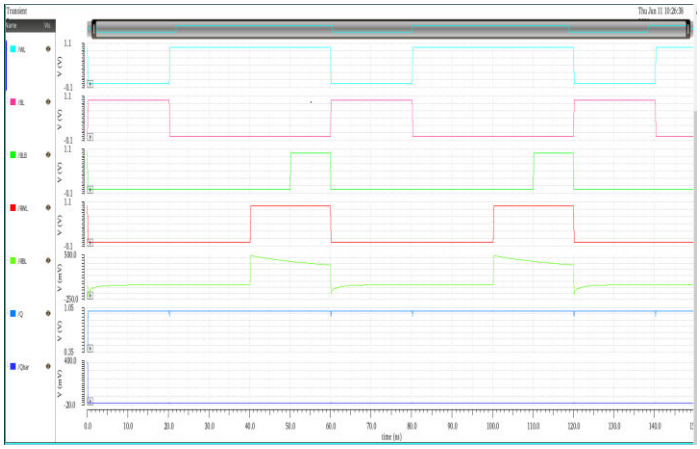
VTH Adjustment: This necessitates the use of a gate work function or Lc tuning, and VTH control is not achievable with a multi fin device with a high aspect ratio.Bulk FinFET Fringing Capacitances

Because consistent doping is difficult to achieve with traditional methods, parasitic resistance exists.Variability Fin width has a big impact on performance.

IV RESULTS

8T sram a detailed performance comparison with the existing various sram structure is done. schematics are drawn using virtuoso.





Write-Hold-Read 1 Operation

V CONCLUSION

The performance evaluation of 6T and 8T SRAM Cells designs was carried out.The performance criteria were stability, power or current leakage. And also, Static Noise Margin (SNM) and the N-curve metric were used for stability analysis. The N-curve is more preferred for the stability measurement because of the advantages of information the N-curve provides about voltage, current, and power in a single plot.The use of pFinFET as access transistors is to achieve the smallest leakage current at the expense of poor write ability. The read and write paths are isolated which provides high read stability. Results show significant improvements in Static Noise Margin, upto 77.7% reduction in read access times, and upto 65.8% reduction in the leakage current. 8T SRAM cell using Self-controlled Voltage level technique reduces the power consumption upto 75%.

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